A Multi-Cell Cascaded High Frequency Link Inverter with Soft-Switching and Isolation

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***Abstract*—Soft-switching inverters can achieve high efficiencies and low switch *dv/dt* and *di/dt*, but often impose additional stress on the switches due to their resonant behavior. Multi-cell converters, on the other hand, can process high voltages by arranging the switches to share the stress. This paper proposes a buck-boost multi-cell soft-switching inverter with inherent cell voltage-balancing. Both the current and voltage stress are shared by the cells. Soft-switching conditions are achieved for all switching transitions without any need for auxiliary circuitry or clamps. A multiple-winding transformer transfers energy between the terminals and provides galvanic isolation. An analytical study and experimental results on a 1200 W prototype verify the operation of the inverter.**

***Index Terms*—Cascaded H-bridge, high-frequency link, multi-cell inverter, multi-level inverter, partial resonant, soft-switching, zero-voltage switching.**

I. Introduction

HARD-switching Pulse-Width-Modulated (PWM) Power converters are the most common power electronic converters in the industry due to their ruggedness and simplicity [1]. These advantages usually come at the cost of an efficiency drop due to high switching losses and severe Electromagnetic Interference (EMI) due to high *dv/dt* and *di/dt*. Soft-switching schemes and multi-cell structures have been proposed over the past several years to address these implications [1-16]. Soft-switching converters rob the switch of its current and/or voltage at the switching instant to create a soft-transition and eliminate or reduce switching losses. This is often achieved by creating a resonant behavior in the waveforms, which results in a ripple in the switch voltage and current and necessitates higher ratings for the switches, especially at high power ranges [2]. Multi-cell structures and specifically multi-level schemes arrange a plurality of components in a way that the switching stress is divided and switch ratings, *dv/dt*, and/or *di/dt* are reduced. The list of multi-cell structures includes, but is not limited to, the cascaded H-bridge [3], diode clamped converters [4], and flying capacitor [5].

A converter can combine the soft-switching and multi-cell features. A significant amount of attention has been given to three-level dc-dc and dc-ac soft-switching converters [8-13]; however, a large advantage in terms of reduction of voltage stress on switches cannot be obtained with only three levels. In [2], a soft-switching dual-active bridge dc-dc converter uses two series-connected half-bridges to achieve a high voltage on the output. In [7], a resonant high step-down dc-dc converter is proposed that has several half-bridge modules on the input side to accept a high voltage, but it is non-isolated. A multi-level flying capacitor inverter is introduced in [14]. Although this non-isolated inverter benefits from soft-switching for all switches and diodes, each phase leg requires auxiliary circuitry that includes two coupled inductors to lower the semiconductor ratings. Another soft-switching approach that can be applied to multi-cell inverters is the use of the Auxiliary Resonant Command Pole (ARCP) [16-17], but cell voltage balancing analysis of the ARCP inverter is rather complicated. Also, the operation of the auxiliary devices at light and full load conditions are different, and this method requires current zero-crossing detection [1].

A class of partial-resonant Zero Voltage Switching (ZVS) converters that use a parallel *LC* link has been proposed and evolved over the past years [18-24]. These converters do not require any auxiliary or clamp networks to facilitate soft-switching and maintain the soft-switching properties in the entire power range. However, similar to almost every resonant and partial-resonant converter, they impose additional ripple on the switch waveforms and therefore increase the required switch ratings. The multi-cell soft-switching inverter proposed in this paper also uses a high-frequency *LC* link as shown in Fig. 1. Galvanic isolation is realized through a multiple-winding high-frequency transformer that can significantly reduce the overall size and weight of the system. The multi-cell structure on the secondary side allows the output switches to share the current as well as voltage stress. The need for bulky dc link components is eliminated by operating the ac link at a high frequency. The ac voltages on cell capacitors are inherently balanced by the transformer windings. This converter maintains ZVS conditions at every switch turn-on and near-ZVS conditions at every switch turn-off throughout the operating range, thereby decreasing the switching losses and *dv/dt*-induced EMI emissions. The proposed converter does not rely on auxiliary circuitry to achieve soft-switching. Transitioning between buck and boost modes is seamless and does not required a change in the algorithm.

II. The Proposed Inverter

The schematic diagram of the proposed inverter is presented in Fig. 1. There is one low-side semiconductor switch, S_i, on the input side which connects the input source to a winding of a

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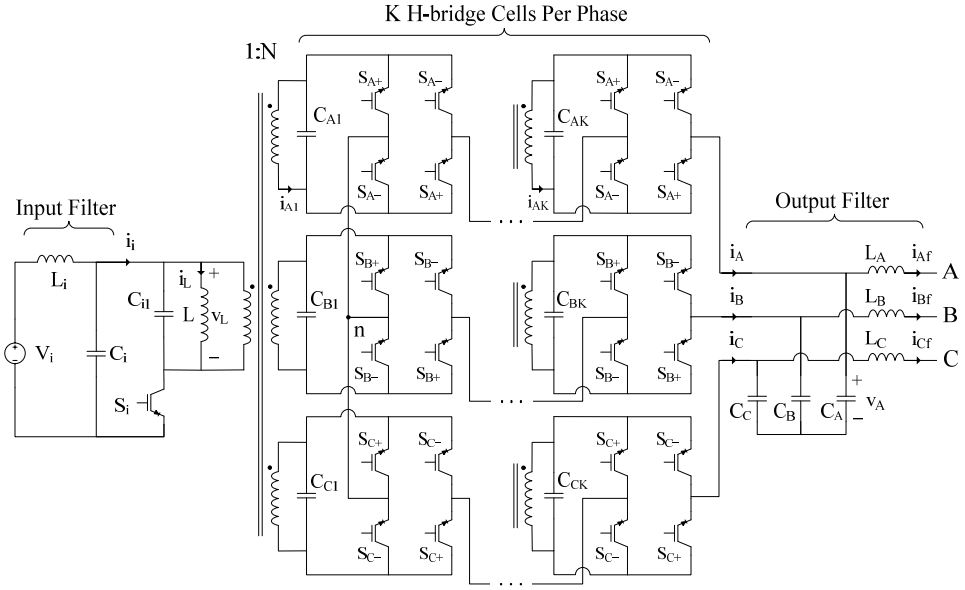

Fig. 1. The proposed soft-switching inverter with cascaded output cells.

multiple-winding transformer. On the output side, each phase is comprised of K series-connected H-bridge cells, each coupled to a transformer winding. All switches conduct unidirectional current and block voltages of both polarities. This can be achieved by using a reverse-blocking switch or simply by putting a diode in series with each switch. The high-frequency transformer has *3K+1* windings, and the turn ratio from the input to an output winding is *1:N*. Each winding is connected in parallel to an ac capacitor, C_{xj}, where x denotes the terminal to which the winding belongs, and j is an index number. For example, C_{AK} is the ac capacitor connected to the K^{th} winding of *phase A*. The magnetizing inductance L and the *3K+1* ac capacitors C_{xj} form a parallel ac link, hereinafter referred to as *the link*. The inductor current i_L and voltage v_L are named the link current and link voltage, respectively. Except for a turn ratio multiplier, the voltage v_L represents the voltage on all link capacitors. Depending on the design requirements, the inverter may have a capacitive or inductive-capacitive filter on its input and output terminals. The latter is the case in Fig. 1 with filter components L_x and C_x. Variable i_i denotes the unfiltered input current as well as the input switch current.

Referring to the output side in Fig. 1, i_x denotes the unfiltered current of phase x and v_x denotes the voltage on filter capacitor C_x. Switches in phase x are named either S_{x+} or S_{x-}. There are only two switch command lines per phase, and switches that receive the same command are given the same name. When S_{x+} (S_{x-}) switches in phase x conduct, the unfiltered phase current, i_x, is positive (negative). As shown in Fig. 1, the leftmost H-bridge cells in the phases are connected to a common point n.

III. Operation of the Inverter

A. Description of the Modes

It was mentioned earlier that the inductance L and the *3K+1* link capacitors, C_{xj}, form a parallel resonant link. An operation cycle of the proposed inverter, $T_{Link}=1/f_{Link}$, is composed of six modes as shown in Fig. 2. The link charges from the input in mode 1, and discharges onto the output phases in modes 3 and

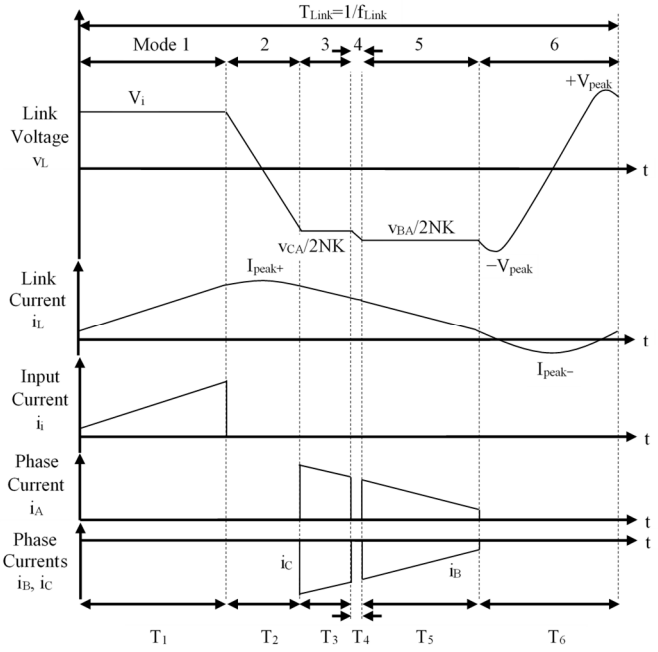

Fig. 2. Operating waveforms and six modes of the proposed inverter. Voltage labels for modes 3 and 5 show an example where $i_{ABC,ref}$= {0.9,−0.1,−0.8} pu and v_{ABC}={0.6,−0.9,0.3} pu.

5. The even-numbered modes 2, 4, and 6 are resonant modes in which no energy transfer occurs. In each link cycle, the controller tries to meet the input dc current reference, $I_{i,ref}$, and the sinusoidal output references $i_{A,ref}$, $i_{B,ref}$, and $i_{C,ref}$. That is, the controller operates the switches in a way that the *average* values of the four currents track their references. The following paragraphs describe the modes, ignoring non-idealities.

Mode 1: In Fig. 3(a), L is charged by the source through S_i. All other switches are in their blocking state. The link voltage, v_L, equals V_i, and i_L increases linearly, as shown in Fig. 2. Once the average input current reference is met, S_i is gated off. In this paper, the *average* value of a variable is calculated over a switching cycle of length T_{link} as indicated in Fig. 2. Due to the presence of S_i between two capacitors C_i and C_{il}, the rate of

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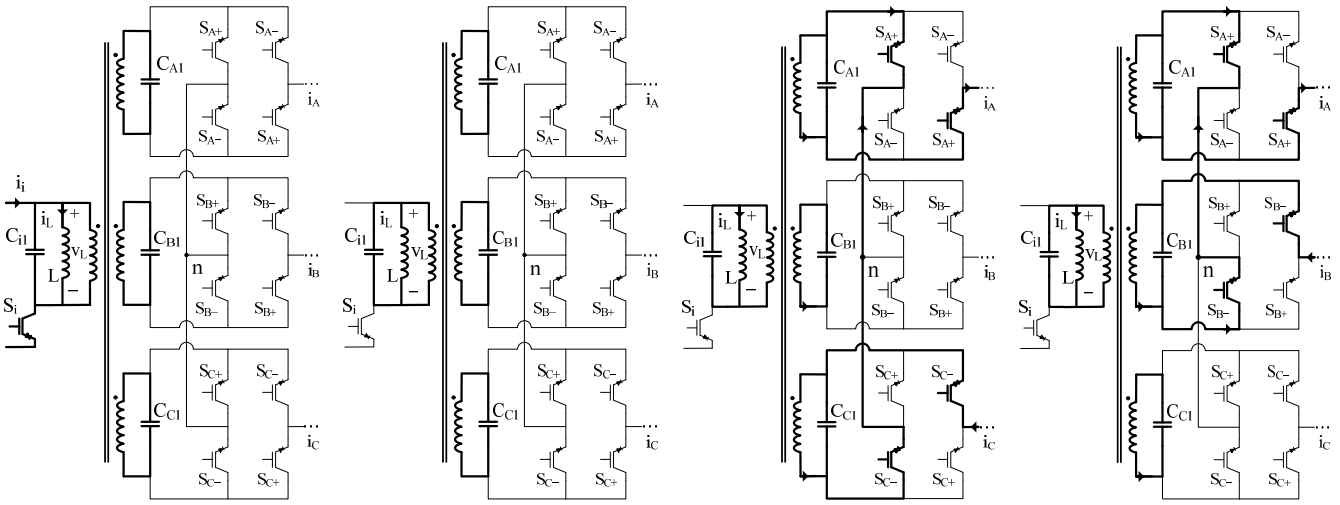

Fig. 3. Current path in different modes. Only one cell per phase is shown. Modes 3 and 5 are shown for an example where $i_{ABC,ref}$= {0.9,−0.1,−0.8} pu and v_{ABC}={0.6,−0.9,0.3} pu.

voltage rise on S_i at turn-off is effectively limited. Therefore, the switch current reduces before its voltage can rise. This near ZVS condition significantly reduces the turn-off loss.

Mode 2: No switches conduct in this mode, therefore the link resonates and v_L changes polarity. The current i_L experiences its positive peak I_{peak+} in this mode. The path of link current is shown in thick lines in Fig. 3(b). On the output side, two phases should be selected to receive energy in mode 3. Out of the three possible phase pairs AB, BC, and AC, the pairs which accommodate the phase with the largest current reference magnitude are candidates for conduction in mode 3. Out of these two pairs, the one with the smaller voltage difference magnitude is selected for mode 3, and the other pair is selected for conduction in mode 5. This leads to a descending link voltage sequence in modes 3, 4, and 5 as shown in Fig. 2, which is an essence in having zero-voltage turn-on. For example, when $i_{ABC,ref}$= {0.9,−0.1,−0.8} pu, and v_{ABC}={0.6,−0.9,0.3} pu, then the pair AC conducts in mode 3, and pair AB conducts in mode 5.

Mode 3: The link is to be discharged on the output pair selected in mode 2. Switches in the selected phase pair should conduct in a way that the polarity of current in the conducting phases matches the polarity of their references. Fig. 3(c) shows the current path for the example made in mode 2. Switches named S_{A+} and S_{C-} conduct in Fig. 3(c) because the current references for phases A and C are positive and negative, respectively. A quick glimpse of Fig. 3(c) proves that a total of *2K* H-bridge cells are connected in series in mode 3, each having a capacitor voltage of Nv_L. Therefore, their aggregate link voltage is $2NKv_L$. The switches of mode 3 start conducting only when they are forward biased, i.e., when their aggregate link voltage matches the pair's instantaneous line-to-line voltage. This means in our earlier example, the switches do not conduct until v_L reaches the value $(v_C-v_A)/2NK$. This ensures zero-voltage turn-on for all conducting switches. i_L reduces linearly as shown in Fig. 2. This mode goes on until one of the conducting phases, namely the phase with the smaller current reference, meets its current reference. In our example, it would be phase C. One may assume that the sinusoidal references are constant within a switching cycle. This carefully designed *end criterion* for mode 3 shapes phase *C* current into a sine wave because the reference current is a sinusoidal. At the end of this mode the switches are gated off. Following the turn-off, the link starts resonating. The voltage rise on the switches happens slowly because of the link capacitors. This allow the switch currents to fall at a near zero voltage and significantly reduces the turn-off loss.

Mode 4: No switches carry current and the link resonates as shown in Fig. 2 and Fig. 3(b). The negative v_L increases in magnitude, until the aggregate link voltage $2NKv_L$ equals the instantaneous line-to-line voltage of the selected output pair of mode 5. In our example, the switches conduct as soon as v_L reaches $(v_B-v_A)/2NK$. Again, this guarantees a zero voltage turn-on for the conducting switches. This ends mode 4 and starts mode 5.

Mode 5: The switches corresponding to the selected pair discharge the link. The selection process of the output pair was explained earlier in mode 2. Similar to mode 5, switches in the conducting phase pair should be selected in a way that the polarity of current in the conducting phases matches their references. Fig. 3(d) shows the current path for our example. Switches named S_{A+} and S_{B-} conduct in Fig. 3(d) because the current references for phases A and B are positive and negative, respectively. Mode 5 continues until the energy in the link drops to a pre-determined level, $E_{desired}$, which will be elaborated later. This mode ends by turning off all switches. Similar to mode 3 following the turn-off, the voltage rise on the switches happens slowly to achieve a near ZVS condition at turn off.

Mode 6: No switches carry current in this mode. With the left-over energy from mode 5 the link resonates and experiences its negative and positive peaks $\pm V_{peak}$. This mode ends when the v_L equals V_i. This is a perfect moment for S_i to turn on at zero voltage. After mode 6, the converter starts mode 1.

The control block diagram of the proposed inverter is depicted in Fig. 4. The controller's main task is to monitor the *end criteria* for the modes. The Moving Average blocks in the

diagram calculate the area below their input waveform. These integrators are reset to zero periodically at the end of their corresponding modes. The block diagram also indicates the controller requires samples of five currents, namely i_i, i_A, i_B, i_C, and i_L. However, it does not imply that five current sensors are required. This is because the waveforms of i_i, i_A, i_B, i_C are actually included in the waveforms of i_L, as indicated in Fig. 2.

B. Considerations

Since the link inductor is separated from the output and input terminals during the charge and discharge modes, respectively, the inverter is inherently a buck-boost converter. The inverter operates in buck mode when $|v_L|$ in mode 5 is smaller than V_i. Otherwise it is considered a boost inverter. The inverter operation and control in both cases are identical.

The input switch, S_i, operates at f_{Link}. The output switches belonging to the phase with the largest current reference switch at $2f_{Link}$ because they conduct in modes 3 and 5, whereas other switches operate at f_{Link} because they conduct in mode 3 or 5.

The link energy at any point in time, E, is defined as:

$$E = \frac{1}{2}C_{tot}v_L^2 + \frac{1}{2}Li_L^2, \tag{1}$$

where C_{tot} is the total link capacitance as seen from the input winding. Assuming that all output-side link capacitors have the same value as C_{A1}, C_{tot} is:

$$C_{tot} = C_{i1} + 3KN^2C_{A1}. \tag{2}$$

It was mentioned in the description of mode 5 that the requirement to end this mode is that the total link energy in the link reduce to a desired level $E_{desired}$. This guarantees that the same amount of energy that was delivered to the link in mode 1 leaves the link in modes 3 and 5, thereby indirectly balancing the input and output power in every cycle.

The link resonant frequency in modes 2, 4, and 6 is:

$$\omega_{res} = 1/\sqrt{LC_{tot}}. \tag{3}$$

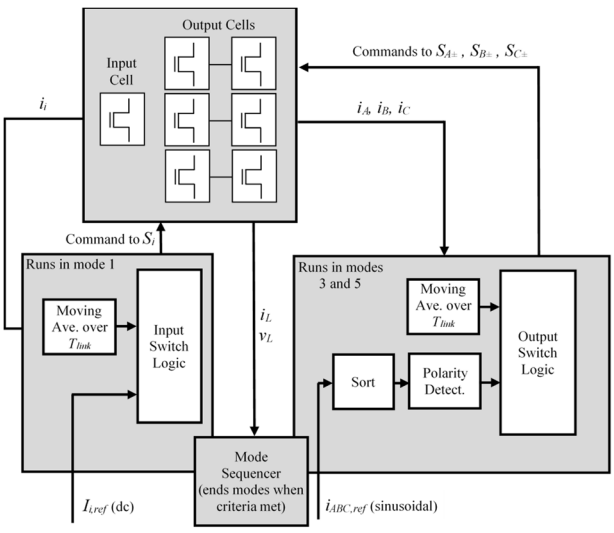

Fig. 4. Control block diagram of the proposed inverter.

Since no power is transferred to the output in mode 6, the link energy in this mode remains essentially constant. The link peak voltages, $\pm V_{peak}$ is:

$$V_{peak} = \sqrt{2E_{desired}/C_{tot}}. \tag{4}$$

It is recommended to use the lowest possible value for $E_{desired}$ and V_{peak}. This is because a large V_{peak} requires a higher voltage rating for the components, makes modes 6 too lengthy. A small V_{peak}, on the other hand, may make mode 6 too short for the digital controller to detect the end of mode 6. Care must be taken on selection of $E_{desired}$ when the inverter operates as a buck inverter. In this case according to mode 6 in Fig. 2, v_L should travel from a smaller value to a larger value, V_i. If there is not enough energy in the link, it can never reach V_i, and ZVS will not be achieved at the turn-on of S_i. In boost mode, however, V_{peak} is greater than V_i by definition. Therefore regardless of buck or boost operation, V_{peak} should not be smaller in magnitude than the greater of V_i and $|v_L|$ of mode 5.

IV. Inverter Design Considerations

A. Analysis of the Inverter

This establishes a relation between the link parameters, the point of operation, ratio N, and key variables such as f_{Link} and I_{peak+}. The following assumptions are made during this analysis:

- Since v_L is essentially constant in charge and discharge modes all link capacitor currents are almost zero and thereby ignored.
- In resonant modes, winding resistances are ignored because they are much smaller than the impedances of link capacitors.
- Voltage ripples on the filter capacitors and voltage drop on the switches are ignored. Unless mentioned otherwise, variable t in the equations of a mode is the time elapsed since the start of the mode. Initial conditions for i_L and v_L at the start of mode m are denoted by $I_{m,0}$ and $V_{m,0}$, respectively.
- As shown in Fig. 2, mode 4 is very short and therefore modes 3 and 5 are assumed combined. The v_L in modes 3 and 5 is a function of time and repeats every π/3 radians. However, the average v_L in the combined mode, $V_{3,5}$ is:

$$V_{3,5} = \frac{3\hat{V}_o}{2\pi K}\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}}\left[\cos\theta - \frac{\cos(\theta+2\pi/3)+\cos(\theta-2\pi/3)}{2}\right]d\theta = \frac{1.432}{2K}\hat{V}_o, \tag{5}$$

where $\hat{V}_o$ is the output peak phase voltage. The link period is:

$$T_{Link} = \frac{1}{f_{Link}} \approx T_1 + T_2 + (T_3 + T_5) + T_6. \tag{6}$$

Assuming that the resistance of the input winding and switch are $R_{w,i}$ and $Rs_{w,i}$, respectively, the link voltage and current for mode 1 are readily derived.

$$\begin{cases} v_L(t) = V_i - (R_{sw,i} + R_{w,i})i_L & (7) \\ i_L(t) = \dfrac{V_i}{R_{sw,i}+R_{w,i}} + \left(I_{1,0} - \dfrac{V_{in}}{R_{sw,i}+R_{w,i}}\right)e^{-\frac{R_{sw,i}+R_{w,i}}{L}t} & (8) \end{cases}$$

Since no switches conduct during resonant modes 2 and 6, the link reduces to a second order LC circuit. Taking i_L and v_L

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as state variables, the following equations are derived from the equivalent circuit:

$$i_L + C_{tot} L \frac{d^2 i_L}{dt^2} = 0 \tag{9}$$

$$v_L(t) = L \frac{di_L}{dt}. \tag{10}$$

From (9) and (10), the solution to link variables during resonant modes is:

$$\begin{cases} i_L(t) = I_{m,0} \cos(\omega_{res} t) + V_{m,0} \sqrt{C_{tot}/L} \sin(\omega_{res} t) & (11) \\ v_L(t) = -L\omega_{res} I_{m,0} \sin(\omega_{res} t) + V_{m,0} \cos(\omega_{res} t). & (12) \end{cases}$$

Similar to mode 1, and assuming output winding and switch resistances of $R_{sw,o}$ and $R_{w,o}$ for each output-side winding, in the combined modes 3 and 5 the link equations are:

$$\begin{cases} v_L(t) = -\frac{V_{3,5}}{2NK} - \frac{2R_{sw,o} + R_{w,o}}{2N^2 K} i_L & (13) \\ i_L(t) = \frac{-V_{3,5} N}{2R_{sw,o} + R_{w,o}} + \left(I_{3,0} + \frac{V_{3,5} N}{2R_{sw,o} + R_{w,o}} \right) e^{\frac{-2R_{sw,o} + R_{w,o}}{2N^2 KL} t}. & (14) \end{cases}$$

So far the equations for i_L and v_L in every mode are obtained. These equations, together with the description of modes lead to a set of simultaneous equations presented by (15-19). Unknowns are T_1, T_2, T_3+T_5, T_6, and $I_{1,0}$. Equations for the undefined $V_{m,0}$ and $I_{m,0}$ are listed in the Appendix. Equations (15-19) are, in order: current reference requirement at mode 1, voltage requirement at the end of mode 2, link energy requirement at the end of the combined modes 3 and 5, voltage requirement at the end of mode 6, and current symmetry at start of mode 1 and end of mode 6. Once a solution is obtained, I_{peak+} can be derived from (20).

$$\begin{cases} I_{i.ref} T_{Link} = \frac{V_i}{R_{sw,i} + R_{w,i}} T_1 \\ \quad + \frac{L}{R_{sw,i} + R_{w,i}} \left(I_{1,0} - \frac{V_i}{R_{sw,i} + R_{w,i}} \right) \left(1 - e^{-\frac{R_{sw,i} + R_{w,i}}{L} T_1} \right) & (15) \\ V_{3,0} = -L\omega_{res} I_{2,0} \sin(\omega_{res} T_2) + V_{2,0} \cos(\omega_{res} T_2) & (16) \\ \frac{1}{2} \times \left(L I_{6,0}^2 + C_{tot} V_{6,0}^2 \right) = E_{desired} & (17) \\ V_{1,0} = -L\omega_{res} I_{6,0} \sin(\omega_{res} T_6) + V_{6,0} \cos(\omega_{res} T_6) & (18) \\ -I_{1,0} = I_{6,0} \cos(\omega_{res} T_6) - V_{6,0} \sqrt{C_{tot}/L} \sin(\omega_{res} T_6) & (19) \end{cases}$$

$$\frac{1}{2} L I_{peak+}^2 = \frac{1}{2} \times \left(C_{tot} V_{2,0}^2 + L I_{2,0}^2 \right) \tag{20}$$

Fig. 5 presents the converter design plots at the input voltage of 150 V, output line to line voltage of 480 V^{rms}, and output power of 1200 W. Selected values for C_{tot} in the plots are 120, 170, and 220 nF. The plots in this figure are valuable during the design phase because they show the effects of three parameters, namely L, N, and C_{tot} on I_{peak+} and f_{Link}. The link peak current determines the transformer's maximum flux, transformer core loss, and the current rating of the input and output switches. I_{peak+} changes only slightly as C_{tot} increases. This is expected because the link capacitors are only in charge of providing soft-switching conditions for the semiconductors. A larger value for C_{tot} results in a slightly larger I_{peak+} because it supplies more energy to the link inductor during mode 2. N and L affect I_{peak+} as well; however, the effect of N is more significant. When current rating of the input switch (and therefore I_{peak+}) is the concern, smaller values of N are more favorable.

Fig. 5 also depicts f_{Link} against L and N for three different values of C_{tot}. f_{Link} is the key variable of this inverter mainly because it determines the sampling time of the digital controller, controls transformer core loss, and affects the size of terminal filters. The effect of C_{tot} is considerable only on the duration of the resonant modes, i.e., T_2, T_4, and T_6. That is why the f_{Link} is not sensitive to the variation in C_{tot}. L, on the other hand, has a substantial effect on f_{Link} due to its active role in determining the duration of every mode. A larger L lengthens every mode and reduces the f_{Link}. In addition, an increase in N prolongs the discharge modes 3 and 5 and reduces the link frequency because the link discharge voltage in these modes, $V_{3,5}/2NK$, is inversely proportional to N.

The above discussion suggests that smaller values for L, N, and C_{tot} are generally more favorable as they lead to higher values for f_{Link} as well as the switching frequency. An increase in the switching frequency, especially in a soft-switching converter, is welcome because it reduces the size of filter components and results in smoother terminal waveforms. Nonetheless too small values for L, C_{tot}, and N necessitate a digital controller with a very high sampling frequency. Fig. 6 shows the contour plots of I_{peak+} and f_{Link} for different values of

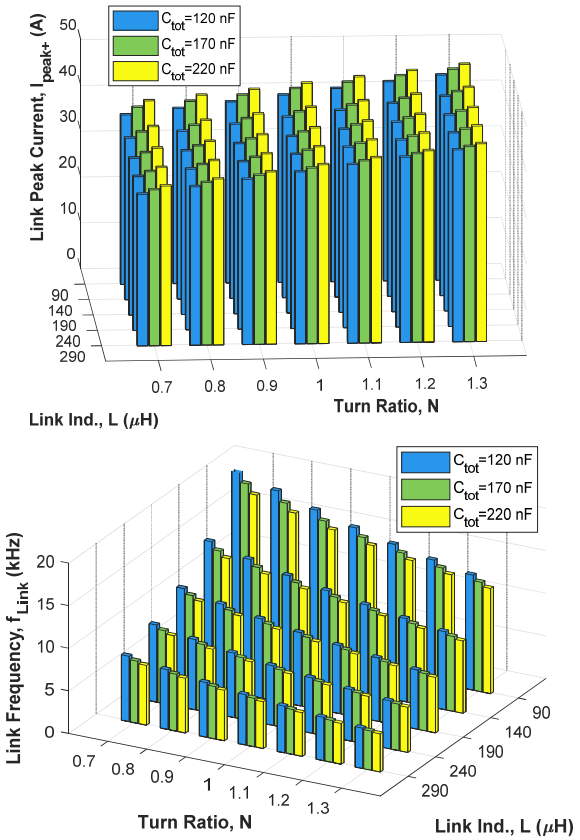

Fig. 5. Link peak current (top) and link frequency (bottom) for various values of N, L, and C_{tot} for V_i=150 V, V_{LL}=480 V at 1200 W.

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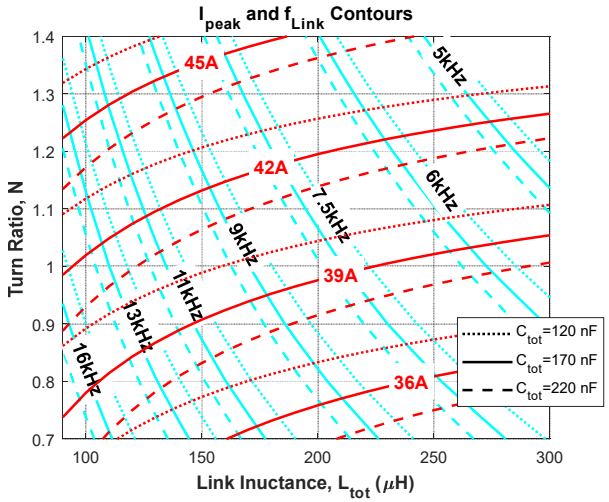

Fig. 6. Contours of f_{Link} and I_{peak+} for V_i=150 V, V_{LL}=480 V at 1200 W.

C_{tot} at the same terminal values as that of Fig. 5. The significance of this plot is that it offers almost all important parameters and variables of the inverter within the same graph.

B. Switch Voltage and Current Stress

Although resonant and partial resonant converters exhibit a superior performance over hard-switching converters in terms of switching losses and EMI emissions, they often result in a higher stress on the components and semiconductor devices. The most notable advantage of having a cascaded series of H-bridge cells in the proposed inverter is the reduction the voltage and current ratings of the output switches.

The maximum current through an output switch happens in mode 3. According to Fig. 3(c), the link inductor is discharged through *2K* H-bridge cells. Each cell receives one over $2K^{\text{th}}$ of i_L. Making a conservative assumption that the current at the start of mode 3, $I_{3,0}$, is almost equal to the link peak current I_{peak+}, the maximum current that an output switch has to conduct is:

$$I_{stress} = \frac{I_{peak+}}{2NK}. \tag{21}$$

The maximum voltage stress on an output-side switch, V_{stress}, happens in mode 6. A KVL equation on the loop shown in thick lines in Fig. 3(c) finds this voltage as a function of time:

$$\begin{aligned} V_{stress} &= \frac{1}{2N}V_{peak} + \frac{1}{2K}\hat{V}_o \sin(\omega_o t), 0 < \omega_o t < \pi, \\ V_{stress} &= \frac{-1}{2N}V_{peak} + \frac{1}{2K}\hat{V}_o \sin(\omega_o t), -\pi < \omega_o t < 0. \end{aligned} \tag{22}$$

where ω_o is the phase angular frequency and t is time elapsed after an appropriate reference. It was mentioned earlier that under boost operation, V_{peak} can be equal to v_L of mode 5. In reference to Fig. 2, the maximum absolute value for v_L in mode 5 is the one over $2K^{th}$ of the peak line-to-line voltage. Therefore, one can rewrite (22) for boost mode as:

$$\begin{aligned} V_{stress} &= \frac{1}{2K}\hat{V}_o\left(\frac{\sqrt{3}}{2N}+\sin(\omega_o t)\right), 0 < \omega_o t < \pi, \\ V_{stress} &= \frac{1}{2K}\hat{V}_o\left(-\frac{\sqrt{3}}{2N}+\sin(\omega_o t)\right), -\pi < \omega_o t < 0. \end{aligned} \tag{23}$$

Equations (21, 23) show that the voltage and current stress on the output-side switches decrease as K increases.

C. Leakage Inductances and Current Sharing

In certain multiple-winding topologies where the magnetizing inductance discharges onto several output windings, the leakage inductances may disturb the balance in current sharing among the windings. This problem, however, does not exist in the inverter proposed in this paper due to the presence of the link capacitors. Prior to conduction of the output switches, the leakage inductances are dominated by the large impedances of the link capacitors, C_{xK}. In the experiments of this paper the typical values for the output winding leakage impedance, $\omega_{res}L_{lK}$, and the link capacitor impedance, $1/\omega_{res}C_{xK}$, are 1.1 Ω and 1333 Ω, respectively.

D. Loss Analysis

The proposed inverter takes advantage of soft-switching at every switching transition for all semiconductor devices. As a result, the major contributing factors to the power loss are the semiconductor conduction loss, transformer conduction loss, and transformer magnetization loss. The inverter's governing equations (15-19) developed earlier are employed to find the three major loss values. The loss created by the input device is:

$$P_{sw,i} = I_{sw,i}^{av}V_{d,i} + (I_{sw,i}^{rms})^2 R_{sw,i}, \tag{24}$$

where $I_{sw,i}^{av}$ and $I_{sw,i}^{rms}$ denote average and rms currents of S_i, and $V_{d,i}$ is the dc voltage drop on the input device.

The equations for all average and RMS currents are included in the appendix. It is worth mentioning that the input and output switches do not inflict losses in the even-numbered resonant modes because they would be in their blocking state. In a similar way, the total loss due to the output devices is:

$$P_{sw,o} = 3 \times K \times 4\left[I_{sw,o}^{av}V_{d,o} + (I_{sw,o}^{rms})^2 R_{sw,o}\right], \tag{25}$$

where $I_{sw,o}^{av}$ and $I_{sw,o}^{rms}$ denote the average and RMS values of the current through an outputs switch, and $V_{d,o}$ is the dc drop on an output device.

All transformer windings experience power loss during resonant modes. However, since resonant modes 2 and 4 are too short, and because the link current in resonant mode 6 is very small, the winding loss to due resonant modes is insignificant. Another factor that makes this loss small is the fact that the link current in resonant modes is split among all *3K+1* windings of the transformer. The input winding carries all the input power in charge mode 1, and therefore has the highest RMS current among the windings. The input and total output winding losses, including the insignificant resonant mode losses, are given by:

$$P_{w,i} = (I_{w,i}^{rms})^2 R_{w,i}, \tag{26}$$

$$P_{w,o} = 3 \times K (I_{w,o}^{rms})^2 R_{w,o}, \tag{27}$$

Where $I_{w,i}^{rms}$ and $I_{w,o}^{rms}$ denote the RMS current through the input and an output winding, respectively.

The transformer core loss in the proposed inverter can be calculated using the Improved Generalized Steinmetz Equation (iGSE) presented by [25]:

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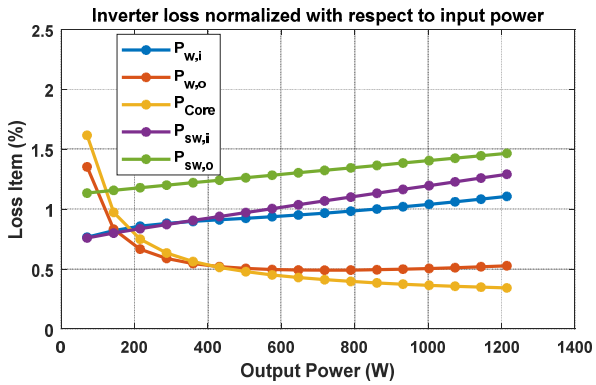

Fig. 7. Calculated loss items for the inverter of Table II.

$$P_{Core} = \frac{V_{core}}{T_{link}} \int_0^{T_{link}} k_i \left|\frac{dB}{dt}\right|^{X_m} (\Delta B)^{Y_m - X_m} dt, \tag{28}$$

$$k_i = \frac{C_m}{(2\pi)^{X_m - 1} \int_0^{2\pi} |\cos\theta|^{X_m} 2^{Y_m - X_m} d\theta}. \tag{29}$$

where ΔB is the peak-to-peak flux density in the core, V_{core} is the ferrite core volume and the three parameters C_m, X_m, and Y_m can be extracted from loss curves provided by the manufacturer. The flux density waveform, $B(t)$, can be derived from $i_L(t)$ through (8), (11), and (14). According to the above discussion, the total power loss in the inverter is estimated by:

$$P_{loss,tot} = P_{sw,i} + P_{sw,o} + P_{w,i} + P_{w,o} + P_{core}. \tag{30}$$

During the design of the inverter, one should note that the input winding and input switch carry several times the RMS current that the output winding and switches conduct. Considering that this inverter can generally be used as a step-up inverter, utilization of a low voltage input switch with a high current rating such as Silicon or Silicon-Carbide MOSFETs is very appropriate.

The plot of calculated power loss for the converter of Table I is presented in Fig. 7. According to this figure, at high power points of operation, most of the loss is caused by the input and output switch conduction losses. At lower power points, however, the transformer core and conduction losses outweigh other losses. This is attributed to the increased link frequency at low powers (*c.f.* Fig. 5) which in turn amplifies the skin effect as well as the core loss.

It was mentioned earlier that the leakage inductances of the output windings do not interfere with the soft-switching. This makes the design of transformer easy in terms of winding arrangements. Routing of the windings near the core gap should be avoided by using a spacer to prevent an increase in the effective resistance due to the fringing magnetic field [26]. When calculating the winding resistances during the design phase, skin and proximity effects should be accounted for properly. While there are several papers dedicated to account for skin and proximity effects in magnetic components [27,28], an interested reader may use the method developed in [29] to calculate the effective resistance values. This method is properly applicable here because the performance of the multiple-winding transformer in the proposed topology is similar to that of a multiple-winding inductor.

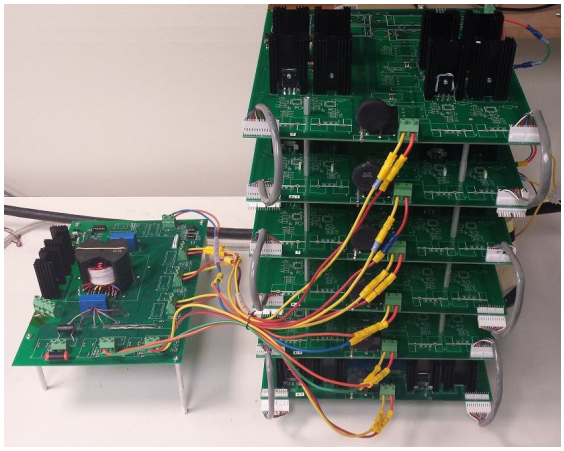

Fig. 8. Photograph of the inverter.

TABLE I
INVERTER AND COMPONENT SPECIFICATIONS AND NOMINAL VALUES

Output Power	1200 W
Input Voltage (V_i)	150 V
Line Output Voltage (V_{LL})	480 V^{rms}
Output Frequency	60 Hz
Link Inductance (L)	110 µH
Number of Cascaded Cells (K)	2
Total Link Capacitance (C_{tot})	120 nF
Link Resonant Frequency ($\omega_{res}/2\pi$)	43.8 kHz
Input Filter (L_i, C_i)	10 µH, 1 mF
Output Filter (L_x, C_x)	0 µH, 5 µF
Input Switch (S_i)	STW72N60DM2AG
Output Switches (S_{x+}, S_{x-})	STW75NF30
Transformer Core, Turn Ration (N)	PM-87×70, 1
Digital Controller	TMS320F28335

V. EXPERIMENTAL RESULTS

A 1200 W setup with two H-bridge cells per phase (K=2) is built to verify the operation of the proposed inverter as depicted in Fig. 8. The inverter specifications and component values are listed in Table I. The link current and voltage along with the unfiltered input current are shown in Fig. 9(a). The measured link frequency and link peak current are 13.2 kHz and 44.5 A, respectively. The values predicted by Fig. 5 are 12.6 kHz and 42.5 A. By examining the waveform v_L, one can verify that the link discharge voltage is smaller in magnitude than the link charge voltage. This indicates that individual cells are operating in *buck mode*. Another example of buck and boost modes will be presented later. In Fig. 9(b), the unfiltered phase currents i_A, i_B, and i_C are depicted. This plot matches the theoritical plot of Fig. 2 in which phase A has the biggest instantaneous current reference and therefore conducts in both modes 3 and 5. Phases C and B conduct only in modes 3 and 5, respectively.

Fig. 10 shows the input and output switch waveforms. Due to the resonance of the link in even-numbered modes, all switches turn on at zero voltage. Also, the presence of link capacitors in parallel with every winding creates near ZVS

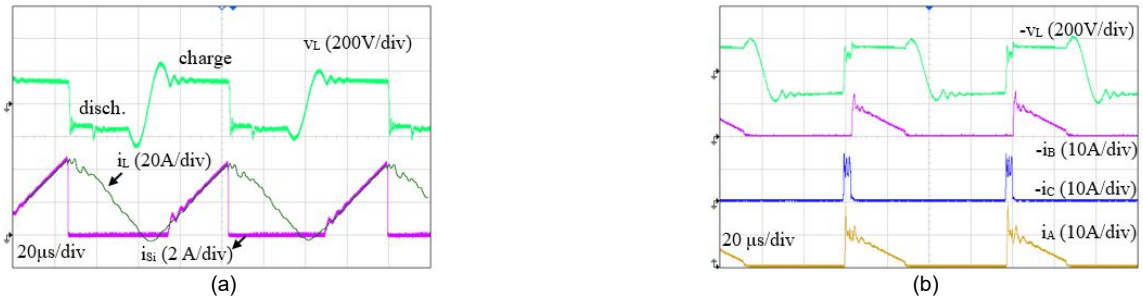

Fig. 9. Switching waveforms at operating conditions of Table I; (a) Link current, link voltage and unfiltered input current; (b Unfiltered phase currents i_A, i_B, and i_C and link voltage.

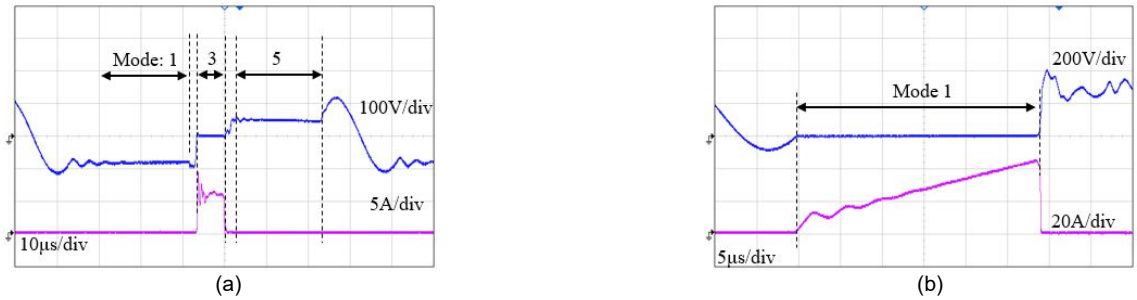

Fig. 10. Switch waveforms; (a) input switch; (b) output switch.

conditions at turn-off of all switches. The leakage inductances of the transformer result in oscillations in the link and switch waveforms. However, they do not interfere with the soft-switching of the semiconductor devices.

The sinusoidal three-phase currents generated by the inverter and the line-to-line voltage waveform are presented in Fig. 11(a) at an output power of 1200 W and unity power factor. The measured current THD is 3.75%. In Fig. 11(b), the inverter supplies 1100 W to a load with a lagging power factor of 85%. The measured current THD is 2.5%. Similarly, the inverter in Fig. 11(c) supplies 640 W to a load with a leading power factor of 74% and the current THD is measured to be 2.3%. The three plots in Fig. 11 verify that the proposed inverter is capable of shaping sinusoidal currents at different power factors and power levels.

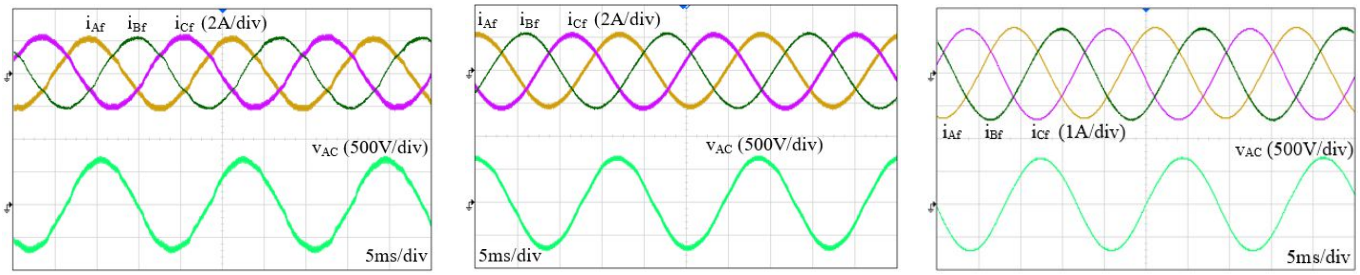

Fig. 11. Output currents and line-t-line voltage; (a) at 1200 W and unity power factor; (b) at 1100 W and 85% lagging power factor; (c) at 640 W and 74% leading power factor.

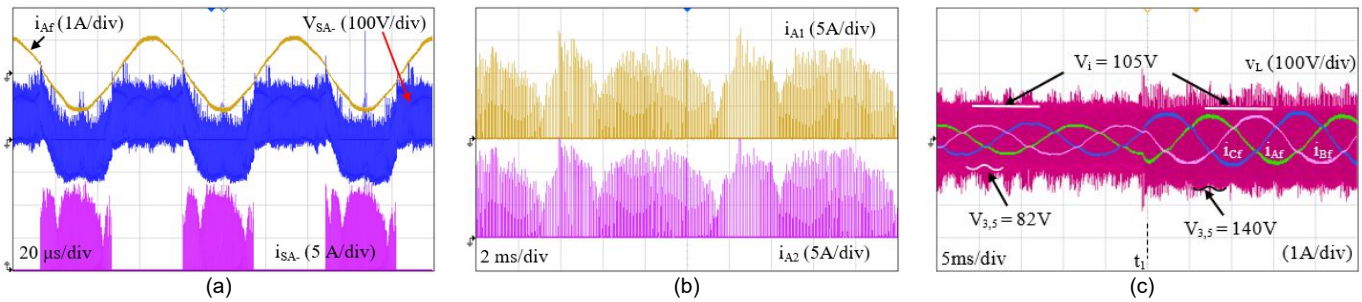

Fig. 12. Inverter waveforms; (a) Output phase current, switch voltage and switch current at operating conditions of Table I; (b) Windings A_1 and A_2 currents; (c) Transitioning from buck to boost mode at time t_1. In buck mode, the discharge voltage, $V_{3,5}$, is smaller than the charge voltage, V_i.

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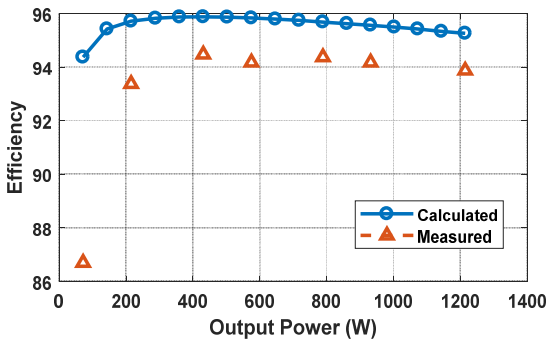

Fig. 13. Measured and calculated efficiency.

Fig. 12(a) shows phase A output current and switch S_{A-} voltage and current. The predicted value for maximum output switch voltage from (22) for V_{peak}=210 V is 203 V which matches the experimental results. The current stress is predicted by (21) to be 11 A. The measured current stress is, however, about 13 A due to the oscillations caused by the transformer and wire leakage inductances.

In Fig. 12(b) the winding currents through cells 1 and 2 of phase A are plotted for a period of output current. The leakage inductances for these two cells are measured to be 6.5 and 3.8 μH, respectively. Although the leakages are significantly different, Fig. 12(b) shows that the current is divided equally between the cells. Therefore, the output cells share the power equally. The efficiency of the converter at V_i = 150 V, V_{LL} = 480 V^{rms}, and unity power factor is measured and reported in Fig. 13.

It was mentioned earlier that in Fig. 9(a), the cells operate in buck mode. If the requested output voltage by the load is small, the cells may operate in buck mode individually (the total output voltage may still be greater than the input voltage due to existence of more than one cell per phase). Fig. 12(c) shows the link voltage and phase for both buck and boost modes. The operation and control of the converter in boost and buck modes are identical. In Fig. 12(c) the inverter operates at an input voltage of V_i = 105 V and transitions from buck mode to boost mode at time t_1. The output line voltages before and after t_1 are 280 V^{rms} and 480 V^{rms}, respectively.

VI. Conclusion

An inverter with a single input-side switch and cascaded output-side switch cells was introduced. Power conversion is realized in a single stage using a partially resonating link. The cascaded output cells allow for the utilization of switches with smaller current and voltage ratings to achieve higher powers. Isolation is provided through a high-frequency multiple-winding transformer. Soft-switching is achieved at turn-on and turn-off transition for all switching devices. A loss model is developed to identify the contributors to the loss. Details of the operation were studied, and experimental results were included.

Appendix

Equations for $V_{m,0}$ and $I_{m,0}$ used in (15-19) are listed below.

$$R_i = R_{sw,i} + R_{w,i} \tag{33}$$

$$R_o = 2R_{sw,o} + R_{w,o} \tag{34}$$

$$I_{2,0} = \frac{V_i}{R_i} + \left(I_{1,0} - \frac{V_i}{R_i}\right) e^{-\frac{R_i}{L}T_1} \tag{35}$$

$$V_{2,0} = V_i - (R_i)I_{2,0} \tag{36}$$

$$I_{3,0} = I_{2,0}\cos(\omega_{res}T_2) + V_{2,0}\sqrt{C_{tot}/L}\sin(\omega_{res}T_2) \tag{37}$$

$$V_{3,0} = -L\omega_{res}I_{2,0}\sin(\omega_{res}T_2) + V_{2,0}\cos(\omega_{res}T_2) \tag{38}$$

$$I_{6,0} = \frac{-V_{3,5}N}{R_i} + \left(I_{3,0} + \frac{V_{3,5}N}{R_i}\right) e^{-\frac{R_i}{2N^2KL}(T_3+T_5)} \tag{39}$$

$$V_{6,0} = -\frac{V_{3,5}}{2NK} - \frac{R_o}{2N^2K}I_{6,0} \tag{40}$$

Equations for the switch and winding currents are listed here.

$$I_{sw,i}^{av} = f_{Link} \times [XT_1 + \frac{L}{R_i}(I_{1,0} - X)\left(1 - e^{-\frac{R_i}{L}T_1}\right)] \tag{41}$$

$$X = \frac{V_i - V_{d,i}}{R_i} \tag{42}$$

$$\begin{aligned}\left(I_{sw,i}^{rms}\right)^2 = f_{Link} \times [X^2T_1 + \frac{2LX}{R_i}(I_{1,0} - X)\left(1 - e^{-\frac{R_i}{L}T_1}\right) \\ +(I_{1,0} - X)^2 \times \frac{L}{2(R_i)}\left(1 - e^{-2\frac{R_i}{L}T_1}\right)]\end{aligned} \tag{43}$$

$$I_{sw,o}^{av} = \frac{f_{Link}}{6NK}[YT_{3+5} + \frac{2N^2KL}{R_o}(I_{3,0} - Y)\left(1 - e^{-\frac{R_o}{L}T_{3+5}}\right)] \tag{44}$$

$$\begin{aligned}\left(I_{sw,o}^{rms}\right)^2 = \frac{f_{Link}}{12N^2K^2} \times [Y^2T_{3+5} \\ +\frac{4N^2KLY}{R_o}(I_{3,0} - Y)\left(1 - e^{-\frac{R_o}{2N^2KL}T_{3+5}}\right) \\ +(I_{3,0} - Y)^2 \times \frac{N^2KL}{R_o}\left(1 - e^{-\frac{R_o}{N^2KL}T_{3+5}}\right)]\end{aligned} \tag{45}$$

$$Y = -\frac{N}{2K} \times \frac{V_{3,5} - V_{d,o}}{R_o} \tag{46}$$

$$\left(I_{sw,i}^{rms}\right)^2 = \left(I_{sw,i}^{rms}\right)^2 + f_{Link}\left(\frac{C_{i1}}{C_{i1} + 3N^2KC_{A1}}\right)^2 (U_1 + U_2) \tag{47}$$

$$U_1 = \frac{1}{2}\left(I_{2,0}^2 + V_{2,0}^2\frac{C_{tot}}{L}\right)[T_2 + \frac{1}{2\omega_{res}}\sin(2\tan^{-1}\frac{I_{2,0}}{V_{2,0}\sqrt{C_{tot}/L}}) - \frac{1}{2\omega_{res}}\sin(2\omega_{res}T_2 + 2\tan^{-1}\frac{I_{2,0}}{V_{2,0}\sqrt{C_{tot}/L}})] \tag{31}$$

$$U_2 = \frac{1}{2}\left(I_{6,0}^2 + V_{6,0}^2\frac{C_{tot}}{L}\right)[T_6 + \frac{1}{2\omega_{res}}\sin(2\tan^{-1}\frac{I_{4,0}}{V_{4,0}\sqrt{C_{tot}/L}}) - \frac{1}{2\omega_{res}}\sin(2\omega_{res}T_6 + 2\tan^{-1}\frac{I_{4,0}}{V_{4,0}\sqrt{C_{tot}/L}})] \tag{32}$$

$$\left(I_{sw,o}^{rms}\right)^2 = \frac{2}{3}\left(I_{sw,o}^{rms}\right)^2 f_{Link}\left(\frac{NC_{A1}}{C_{i1}+3N^2KC_{A1}}\right)^2 (U_1+U_2) \qquad (48)$$

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